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10/677,191	10/02/2003	Gregory S. Glenn	PD-02-0360/11836 (21797-0	8302

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EXAMINER	
TRINH, THANH TRUC	

ART UNIT	PAPER NUMBER
1753	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/677,191	GLENN, GREGORY S.	
	Examiner	Art Unit	
	Thanh-Truc Trinh	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *30 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 1-15 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable by Glenn (US Patent 6313396) in view of Vilela et al. (US Patent 5800630).

Regarding claim 1, as seen in Figure 1, Glenn discloses a solar cell structure having a solar cell unit structure comprising a heat sink 20; a solar cell (11 or 12 or 13) having a front side 29, a back side 21, a solar cell projected area coverage on the heat sink, wherein the solar cell comprises an active semiconductor structure that produces a voltage between the front side and the back side when the front side is illuminated; and an intermediate structure (including all the layers between solar cells 11, 12, 13 and the heat sink) of disposed between and joined to the back side of the solar cell and to the

heat sink, and having an intermediate structure projected area coverage on the heat sink. The intermediate structure further comprises a by-pass diode 15 having a diode projected area coverage on the heat sink. (See Figure 1 and col. 4 lines 10-31, 62-67 and col. 5 lines 1-19)

Regarding claim 2, Glenn discloses the diode projected area coverage on the heat sink is less than the solar cell projected area coverage on the heat sink, and wherein the intermediate structure further comprises a substrate (bonding element 18, dielectric layer 16, conducting element 17...) coplanar with the by-pass diode 15. (See Figure 1).

Regarding claim 3, Glenn discloses the diode projected area coverage on the heat sink is less than the solar-cell projected area coverage on the heat sink, and the intermediate structure further comprises a substrate (bonding element 18 and dielectric layer 16, conducting element 17...) coplanar with the by-pass diode 15 and having a substrate projected area coverage on the heat sink such that the diode projected area coverage on the heat sink and the substrate projected area coverage on the heat sink taken together are not less than the solar cell projected area coverage on the heat sink. (See Figure 1)

Regarding claim 4, Glenn discloses the diode projected area coverage on the heat sink is less than the solar cell projected area coverage on the heat sink, and the substrate has a substrate notch, and the by-pass diode is received into the substrate notch. (See Figure 1). It is the position of the examiner to consider the "notch" is a region in the substrate to have the diode. Glenn teaches the substrate having a region

for the by-pass diode as shown in Figure 1. Therefore Glenn teaches the limitations of the instant claim.

Regarding claim 5, Glenn discloses the intermediate-structure projected area coverage on the heat sink is not less than the solar cell projected area coverage on the heat sink. (See Figure 1)

Regarding claim 6, Glenn discloses an intra-unit electrical connection structure (planar tab 14) operable to electrically interconnect the solar cell and the by-pass diode in an electrical anti-parallel relation. (See Figures 1).

Regarding claim 7, Glenn teaches the back side of the solar cell is substantially planar. (See Figure 1).

Regarding claim 8, Glenn describes that the solar cell structure includes at least one additional solar cell unit structure as set forth in claim 1, and further including a circuit electrical connection structure (metal trace 19, conducting element 17 and planar tab 14) operable to electrically interconnect each of the solar cell unit structures in series. (See Figure 1).

Regarding claim 9, Glenn disclose a solar structure as described in claim 1, wherein the solar cell structure includes a joint (metal trace 19 and conducting element 17) between the intermediate structure and the heat sink, and wherein the joint comprises a metallic trace deposited upon a dielectric (bonding 18). (See Figure 1 and col. 5 lines 24-26).

Regarding claim 10, Glenn describes that the solar cell structure includes a joint between the intermediate structure and the heat sink. (See Figure 1). The joint

comprises metal trace 19, conducting element 17 and bonding 18. The structure of the joint is indistinguishable to a PC board having a metal trace on a face, therefore the reference teaches the limitation of instant claim.

Regarding claim 11, Glenn discloses a solar cell structure 10 having a solar cell unit structure comprising a heat sink (20); a solar cell (11, 12 or 13); an intermediate structure (layers 15-19 between the heat sink 20 and solar cells 11, 12, and 13); an intra-unit electrical connection structure (tab 14). The solar cell has a front side 29, a back side 21, a projected area coverage on the heat sink, and inherently comprises an active semiconductor structure that produces a voltage between the front side and the back side when the front side is illuminated. The intermediate structure is disposed between and joined to the back side of the solar cell and to the heat sink and having an intermediate-structure projected area coverage on the heat sink. The intermediate structure also comprises a by-pass diode 15 having a diode projected area coverage on the heat sink that is less than the intermediate-structure projected area coverage on the heat sink, and a substrate including layers 16-19 in which layers 16, 17 and 18 are coplanar with the by-pass diode 15. The substrate projected area coverage and the diode projected area coverage on the heat sink taken together are not less than the solar cell projected area coverage on the heat sink. And finally, the intra-unit structure operable to electrically interconnect the solar cell and the by-pass diode in an electrical anti-parallel relation. (See Figure 1 and col. 4 lines 24-31)

Regarding claim 12, Glenn describes the back side of the solar cell is substantially planar. (See Figure 1)

Regarding claim 13, Glenn discloses a solar cell structure further including a circuit electrical connection structure (metal trace 19, conducting element 17) operable to electrically interconnect each of the solar cell unit structures in series. (See Figure 1)

Regarding claim 14, Glenn disclose a solar cell structure as described in claim 11, wherein the solar cell structure includes a joint (metal trace 19 and conducting element 17) between the intermediate structure and the heat sink, and wherein the joint comprises a metallic trace (metal trace 19 or conducting element 17) deposited upon a dielectric layer 18. (See Figure 1 and col. 5 lines 24-26)

Regarding claim 15, Glenn describes that the solar cell structure includes a joint (metal trace 19, conducting element 17 and bonding 18) between the intermediate structure and the heat sink. (See Figure 1). The structure of the joint is not distinguishable to that of a PC board having a metal trace on a face. Therefore, Glenn teaches the limitation of the instant claim.

Regarding claim 21, Glenn describe the by-pass diode is attached by soldering or conductive adhesive. (See col. 4 lines 24-31). Therefore, the by-pass diode is a discrete by-pass diode. (See Figure 1)

Glenn does not specifically teach including a back-side metallization at the back side of the solar cell, but suggests using solar cells such as shown in Vilela et al. (US Patent 5800630). (See col. 4 lines 18-21).

Vilela et al. teach including a back-side metallization at the back side of the solar cell. (See Figure 1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the solar cell structure of Glenn by utilizing back-side metallization as taught by Vilela et al., because it is suggested by Glenn.

1. Claims 1, 5-8 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable by Hartman et al. (US Patent 4577051) in view of Vilela et al. (US Patent 5800630).

Regarding claim 1, as seen in Figures 1-3, Hartman discloses a solar cell structure having a solar cell unit structure comprising a heat sink (22); a solar cell (16) having a front side, a back side, a conductive substrate (15) and a projected area coverage on the heat sink, wherein the solar cell comprises an active semiconductor structure that produces a voltage between the front side and the back side when the front side is illuminated; an intermediate structure (combination of diode body 21, long leg 13 and short leg 14 of conductor strips 12) disposed between and joined to the conductive substrate 15 and heat sink (22). (See col. 3 lines 19-68 bridging col. 4 lines 1-43)

Regarding claim 5, as seen in Figures 1-2, Hartman discloses the intermediate structure (diode body 21, long leg 13 and short leg 14 of conductive strips 12) projected area coverage on the heat sink is not less than the solar cell projected area coverage on the heat sink.

Regarding claim 6, Hartman describes an intra-unit electrical connection structure (soldering or conductive adhesive – See col. 3 lines 38-44) operable to electrically interconnect the solar cell (16) and bypass diode (diode body 21, long leg 13

and short leg 14 of the conductive strips 12) in an electrical anti-parallel relation. (See Figures 1-3 and col. 4 lines 43-58).

Regarding claim 7, Hartman discloses the back side of the solar cell 16 is substantially planar. (See Figures 1-3)

Regarding claim 8, Hartman discloses solar cell structure having more than one solar cell unit as described in claim 1 connected in series. (See Figures 1-3, col. 5 lines 25-36). In order to connect solar cells in series, there must be a circuit electrical connection structure operable to electrically interconnect each of the solar cell unit structures in series. (See col. 5 lines 35-41)

Regarding claim 21, Hartman teaches the bypass diode is a discrete bypass diode. (See Figure 2)

Hartman does not specifically teach the conductive substrate 15 is made of metal, or having a back-side metallization.

Vilela et al. teach a solar cell having a back-side metallization. (See Fig. 1)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Hartman by utilizing a back-side metallization as taught by Vilela et al., because it would give a low resistance back contact. In addition, it is conventional use a metallization layer for back contact or conductive substrate.

2. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable by Hartman et al. (US Patent 4577051) in view of Vilela et al. (US Patent 5800630).

Regarding claim 16, as seen in Figures 1-3, Hartman discloses a solar cell structure having at least two solar cell unit structures, and each solar cell unit comprising a heat sink (22); a solar cell (16) having a front side, a back side, a conductive substrate (15) and a projected area coverage on the heat sink, wherein the solar cell comprises an active semiconductor structure that produces a voltage between the front side and the back side when the front side is illuminated; an intermediate structure (combination of diode body 21, long leg 13 and short leg 14 of conductor strip 12) disposed between and joined to the conductive substrate 15 and heat sink (22), See col. 3 lines 19-68 bridging col. 4 lines 1-43, wherein the intermediate structure comprises a bypass diode (body 21, long leg 13 and short leg 14 of conductive strip 12) having a diode projected area coverage on the heat sink (22) that is substantially the same as the intermediate-structure projected area coverage on the heat sink; an intra-unit electrical connection structure (soldering or conductive adhesive – See col. 3 lines 38-44) operable to electrically interconnect the solar cell and the by-pass diode in an electrical anti-parallel relation. The solar cell unit structures are electrically interconnected in series. (See Figures 1-3, col. 5 lines 25-36). Therefore, there must be a circuit electrical interconnection. (See col. 5 lines 35-41)

Regarding claim 17, as seen in Figures 1-2, Hartman discloses the intermediate structure (diode 21 and conductive strips 12) projected area coverage on the heat sink is not less than the solar cell projected area coverage on the heat sink.

Regarding claim 18, Hartman discloses the back side of the solar cell 16 is substantially planar. (See Figures 1-3)

Hartman does not specifically teach the conductive substrate 15 is made of metal, or having a back-side metallization.

Vilela et al. teach a solar cell having a back-side metallization. (See Fig. 1)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Hartman by utilizing a back-side metallization as taught by Vilela et al., because it would give a low resistance back contact. In addition, it is conventional use a metallization layer for back contact or conductive substrate.

3. Claims 9-10 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable by Hartman et al. (US Patent 4577051) in view of Vilela et al. (US Patent 5800630) and further in view of Glenn (US Patent 6313396).

Regarding claims 9 and 19, Hartman and Vilela et al. disclose a solar cell structure as described as claims 1 and 16. Hartman also describes a joint (20) between the intermediate structure (including diode body 21, long leg 13 and short legs 14 of conductor strips 12) and the heat sink (22). The joint (or diagonal arm 20) is made of very thin copper. (See col. 3 lines 30-35). Therefore it is the Examiner's position that a very thin copper joint is a metallic trace.

Neither Hartman nor Vilela et al. teach the metallic trace deposited upon a dielectric.

Glenn teaches metal trace (19 and 17) deposited upon a dielectric layer 18. (See Figure 1 and col. 5 lines 24-26).

It would have been obvious to one ordinary skill in the art at the time the invention was made to modify the structure of Hartman and Vilela et al. by depositing the metal trace upon a dielectric as taught by Glenn, because it would provide bonding the conductive trace to the solar cell, and further support the solar cell. (See col. 5 lines 5-19).

With respect to claim 10 and 20, in such a combination described in claims 9 and 19, the structure of the copper joint (diagonal arm 20 of Hartman) deposited upon a dielectric layer (18 of Glenn) is not distinguishable from a structure of a PC board having a metal trace on a face. Therefore, it would have been obvious to one skill in the art that metallic trace (20) deposited upon a dielectric layer (18) is the joint comprising a PC board with metal trace on a face.

Response to Arguments

Applicant's arguments with respect to claim 05/30/2007 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues that Glenn does not disclose a heat sink. The substrate 20 in Glenn is made of a dielectric material and cannot perform as a heat sink. The Examiner wants to point out that a dielectric material cannot conduct electricity, not heat. Electricity and heat are two different subject matters. As long as substrate 20 has one surface area for absorbing heat and other surface area for dissipating heat, the Examiner believe that substrate 20 can perform as a heat sink.

Applicant also argues that Glenn does not disclose the limitation "a solar cell having ... a back side ..., wherein the solar cell includes a back-side metallization at the back side; and an intermediate structure disposed between and joined to the back-side metallization of the solar cell and to the heat sink...". The Examiner replies that Glenn suggests using solar cell having back-side metallization by pointing to US Patents 5800630 and 5407491 (See col. 4 lines 12-21). And both US Patents 5800630 and 5407491 teach solar cell having back-side metallization. (See Figure 1 of '630 and '491). Therefore, in the combination of Glenn's disclosure and teaching of either one of US Patents 5800630 or 5407491, the intermediate structure is indeed disposed between and joined the back-side metallization and the heat sink.

Applicant further argues that a PC board and a configuration of elements 17,18 and 19 of Glenn are not the same, and that in PC board the metallic traces are deposited overlying a broad face of a nonconductor. The Examiners respectfully disagrees. Glenn teaches metallic traces 17 and 19 are disposed upon a dielectric (nonconductive) material such as layer 18. Similarly, a PC board has metallic traces deposited on a surface such as a board. Therefore, it is the Examiner's position that the structure of the joint of metallic traces 17 and 19 disposed upon dielectric layer 18 is indistinguishable to that of a PC board having a metal trace on a face.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh-Truc Trinh whose telephone number is 571-272-6594. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

08/15/2007

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